CLAIMS

What is claimed is:

1. A membrane switch circuit layout comprising two or more non-conductive membrane layers, each membrane layer having top and bottom surfaces, a conductive circuit trace printed on the top surface of each membrane layer, a first membrane layer being positioned beneath a second membrane layer, the second membrane layer having thru-holes selectively cut there through and positioned to provide electrical connection between circuit traces printed on the membrane layers.

2. The circuit layout of claim 1 wherein the thru-holes connect the conductive circuit trace printed on the second membrane with the conductive circuit trace printed on the first membrane.

3. The circuit layout of claim 1 wherein conductive ink at least partially fills the thru-holes.

4. The circuit of claim 1 wherein the membranes are electrically insulating.

5. The circuit of claim 1 wherein the second membrane electrically insulates traces printed on its top surface from traces printed on the first membrane.

6. The circuit of claim 1 further comprising an adhesive positioned between first and second membrane layers.

7. The circuit of claim 4 wherein the adhesive is selectively printed for openings on the top surface of the first membrane layer.

8. The circuit of claim 4 wherein the adhesive is selectively printed for openings on the bottom surface of the second membrane layer.

9. The circuit of claim 4 wherein the adhesive is an adhesive layer positioned between first and second membrane layers, the adhesive layer having openings selectively cut there through.

10. The circuit of claim 1 wherein pads for receiving conductive ink are printed on the first membrane layer corresponding to the location of the thru-holes in the second membrane layer.

11. The circuit of claim 1 wherein the first membrane layer is a film layer between 0.001 and 0.007 inches thick.

12. The circuit of claim 1 wherein the second membrane layer is a film layer between 0.001 and 0.007 inches thick.

13. The circuit of claim 1 further comprising a third nonconductive membrane layer having top and bottom surfaces, a conductive circuit trace being printed on the top surface of the third membrane layer, the third membrane layer having thru-holes and being positioned over the second membrane layer to provide electrical connection between the conductive circuit printed on the third membrane layer and the conductive circuit printed on either the second or the first membrane layers.

14. The circuit of claim 13 further comprising an adhesive positioned between second and third membrane layers.

15. A method for constructing a membrane circuit layout having at least two membrane layers, the method comprising the steps of:

printing the top surface of a first membrane layer with a conductive circuit trace;

positioning a second membrane layer having thru-holes selectively cut there through over the first membrane layer; and

printing the top surface of a second membrane layer with conductive circuit traces, the printing being over at least one thru-hole providing an electrical connection between traces on the first and second membrane layers.

16. The method of claim 15 further comprising the step of positioning an adhesive between the first and second membrane layers.

17. The method of claim 16 wherein the adhesive is selectively printed for openings on the top surface of the first membrane layer.

18. The method of claim 16 wherein the adhesive is selectively printed for openings on the bottom surface of the second membrane layer.

19. The method of claim 16 wherein the membranes are electrically insulating.

20. The method of claim 16 wherein the second membrane electrically insulates traces printed on its top surface from traces printed on the first membrane.

21. The method of claim 16 wherein the adhesive is an adhesive layer applied between the first and second membrane layers, the adhesive layer being selectively cut for openings.

22. The method of claim 15 wherein pads for receiving conductive ink are printed on the first membrane layer corresponding to the location of the thru-holes in the second membrane layer.

23. The method of claim 15 wherein the first membrane layer is a film layer between 0.001 and 0.007 inches thick.

24. The method of claim 15 wherein the second membrane layer is a film layer between 0.001 and 0.007 inches thick.

25. The method of claim 15 further comprising the steps of placing a third membrane layer, having thru-holes selectively cut through the third membrane layer, over the second membrane layer; imprinting the top surface of a third membrane layer with conductive circuit traces; and pressing conductive ink through the holes in the second membrane layer.

26. The method of claim 25 further comprising the step of placing an adhesive between the second and third membrane layers.